

**Amendments To The Drawings**

The two (2) attached drawing sheets provide a revised FIG. 6.

One of the attached sheets is annotated using a yellow highlighter to show the proposed corrections to FIG. 6. The other attached sheet is a replacement sheet.

Attachment: Replacement Sheets of FIGS. 4-6

Annotated Sheet Showing Changes of FIGS. 4-6

**REMARKS/ARGUMENTS**

Reconsideration of the above-identified application is respectfully requested.

In the Office Action, the Examiner objected to the drawings as not showing every feature of the invention specified in the claims. In particular, the Examiner contends that the figures as filed do not show: the host identifying pulse width  $T_s$ ; the host releasing pulse width  $T_w$  and the feedback pulse width  $T_r$ , which are recited in claims 1, 3, 6 and 9. The Examiner also contends that the figures do not show a logic OR bus or a simple AND bus.

A revised FIG. 6 is submitted with depicts  $T_r$ . No new matter is added because  $T_r$  is fully described in the specification text. As for showing  $T_s$ , various instances of  $T_s$  are shown in FIG. 6 as filed. In particular,  $T_{s2}$  and  $T_{s3}$  are clearly shown in FIG. 6.

As for  $T_w$ , the Applicant contends that  $T_w$  is not capable of illustration as it is a pulse width time or duration that a slave module responds to. As such,  $T_w$  is analogous to a scalar used for the determination of host releasing. See for example the first full paragraph on page 9. Since  $T_w$  is not capable of being depicted in the figures yet is described in the specification, claims that recite  $T_w$  as a limitation are fully supported by the specification.

Claims 1-9 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 4,886,981 to Lentini et al. The Examiner contends that Lentini et al. describes a synchronized circuit for a plurality of power units, however, the Examiner did not identify where and how Lentini et al. teaches the limitation of claim that requires each of the parallel-connected modules to have different host-identifying  $T_s$  pulse widths and different host-releasing pulse widths  $T_w$ .

FIG. 2 of Lentini et al. describes a synchronizing unit US shown in FIG. 1. (See column 3, lines 52-55.) The circuit shown in FIG. 2 does not provide different output pulse widths. (See column 4, lines 3-13.)


The operation of the circuit shown in FIG. 1 is illustrated in FIG. 4. (See column 5, lines 12-16.) Nowhere in FIG. 4, or anywhere else in Lentini et al. is there any suggestion of outputting different pulse widths to select a master from several slave units as recited in pending claim 1.

Claim 1 and all of the claims that depend on claim 1 are allowable over Lentini. Unless the Examiner can identify by column and line number in Lentini et al. where every limitation of claim 1 is found, the rejection of claim 1 as well as any claim that depends on claim 1, improper and should be withdrawn.

Since many of the limitations of claim 1 are missing from Lentini et al., the Applicants respectfully submits that claims 1-9 are in condition for allowance over the cited references.

Respectfully submitted,

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**APPENDIX OF ATTACHMENTS**

Application Serial No. 10/500,452  
Reply to Office Action of August 8, 2005

**Replacement Sheet of FIGS. 4-6  
(a total of one sheet of drawings)**

and

**Annotated Sheets Showing Changes of FIGS. 4-6  
(a total of one sheet of drawings)**

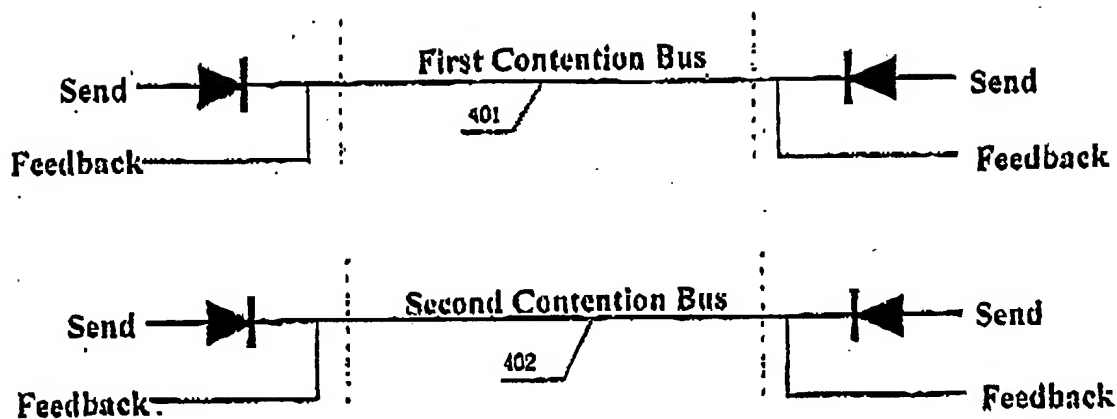


FIG 4

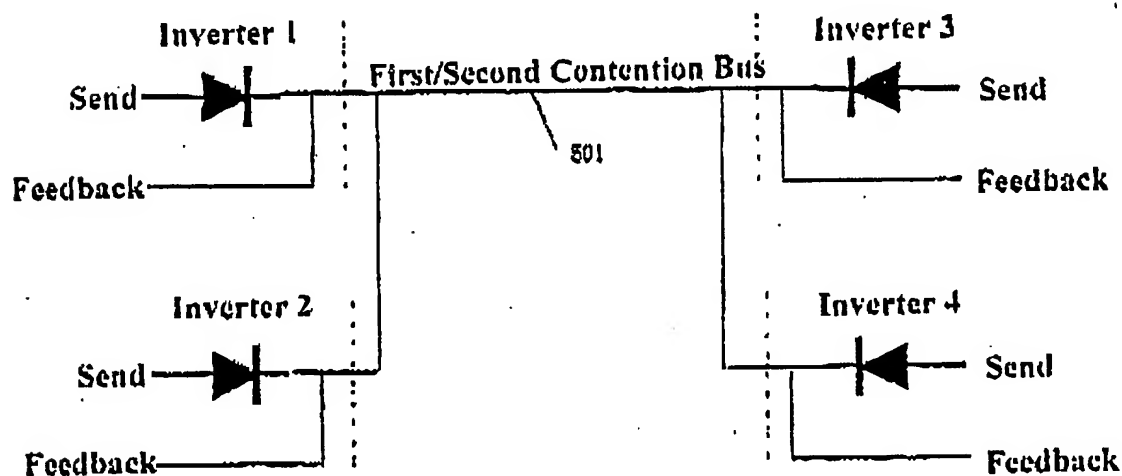


FIG 5

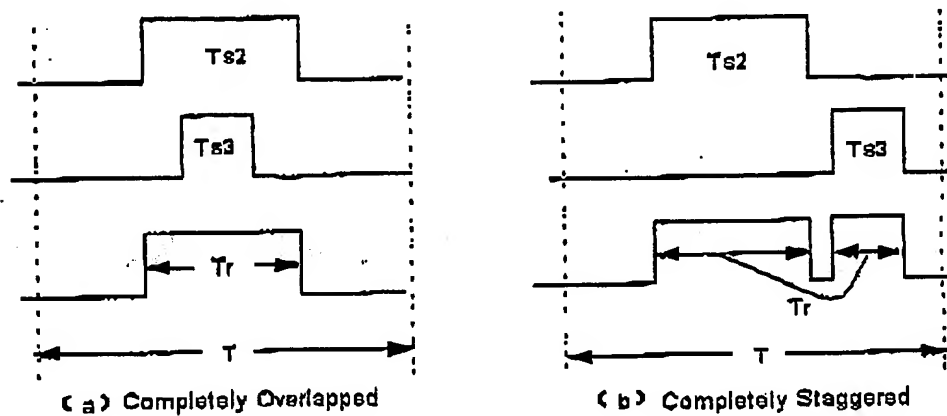


FIG 6